WHAT IS CLAIMED IS

1. A subcode-data generating circuit, which generates subcode data including subcode component data which indicates any one of time information and information other than the time information, said circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the subcode component data which indicates the information other than the time information; and

a selecting portion which selects one of the outputs of said first and second generating portions.

2. The subcode-data generating circuit, as claimed in claim 1, wherein said second generating

portion comprises a plurality of generating portions provided separately.

3. A subcode-data generating circuit, which generates subcode data including subcode component data which indicates any one of time information and information other than the time information, said circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the subcode component data which indicates the information other than the time information;

a selecting portion which selects one of the outputs of said first and second generating portions; and

a memory in which commands for automatic generation of the subcode component data are written,

wherein the commands include first commands for automatic generation of the subcode component data

which indicates the time information, which first commands are written collectively in a first area of said memory, and second commands for automatic generation of the subcode component data which indicates the information other than the time information, which second commands are written collectively in a second area of said memory.

4. The subcode-data generating circuit, as claimed in claim 3, wherein:

said second generating portion comprises a plurality of generating portions provided separately;

said second area of said memory comprises a plurality of areas corresponding to said plurality of generating portions; and

commends of the second commands are written collectively in each area of said plurality of areas, which commands correspond to a respective one of said plurality of generating portions.

5. A subcode-data generating circuit, which generates subcode data including subcode component data, the state of which alternates between a high state and a low state at a predetermined period, said circuit comprising:

a toggle generating portion which independently generates data, the state of which alternates between the high state and the low state at the predetermined period; and

a selecting portion which selects one of the output of said toggle generating portion and data, the state of which alternates between the high state and the low state at the predetermined period based on a number of sectors based on original data of the subcode component data.